IN THE DRAWINGS:

Please replace each of the drawings with the corresponding drawing on the attached Replacement Sheet(s).

REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. Applicant has amended Claims 6, 9 and 10. Applicant submits that no new matter has been added by this amendment. Thus, Claims 6-10 remain pending. This application has been carefully reviewed in light of the Official Action mailed April 11, 2008. Applicant respectfully requests reconsideration and favorable action in this case.

Drawing Objections

The drawings stand objected to as failing to comply with 37 C.F.R. § 1.121(d). Please replace the drawings with the enclosed Replacement Sheets. Annotated Marked-up Drawings, concurrently submitted herewith, include annotations to show the changes to the drawings more clearly.

More specifically, labels have been added to FIGURES 1-20 where appropriate.

Rejections under 35 U.S.C. § 112

Claims 6 and 9-10 stand rejected under 35 U.S.C. § 112, second paragraph. Applicant has amended Claims 6, 9 and 10 and respectfully submits that this rejection is now moot.

Claim 6 stands rejected under 35 U.S.C. § 112, first paragraph. With respect to this rejection of Claim 6, Applicant respectfully submits that "how the second circuit supplies the first circuit with data when the counter signal has a value equal to a common multiple of n and m" is clear from the specification and drawings at least as follows. Take the functional circuit 3 which operates with clock signal CLKb and the functional circuit 3 which operates with clock signal CLKc in FIGs. 6 and 8. Each of counter signals prepared for each of the two functional circuits 3 counts the same counts and has the same phase (See Specification, page 16, lines 12 to 16). Therefore, these counter signals may operate in the same way or may be the same signal and thus the term "the counter signal" will be used to refer to these two counter signals hereinafter,

As discussed in the specification, Clock signal CLKb may have twice the period of clock signal CLK and has a phase which becomes zero every time the counter signal counts a multiple of

2 (See Specification, page 16, line 18 to page 17, line 2). Similarly, clock signal CLKc has a period three times the period of clock signal CLK and has a phase which becomes zero every time the counter signal counts a multiple of 3 (See Specification, page 17, lines 3 to 11). Therefore, clock signals CLKb and CLKc may have the same phase (e.g. zero) every time the counter signal counts a multiple of 6, which is the product of 2 and 3. This means the two functional circuits 3 can successfully carry out communication including data transfer when the counter signal counts a multiple of 6.

Each one of the two functional circuits 3 learns the frequency of a clock signal CLKb or CLKc of the other functional circuit 3 (See Specification page 18, line 19 to page 19, line 5). The information on the frequency of the clock signal can be stored in, for example, a memory circuit. Each functional circuit 3 uses the information and a simple logical circuit to determine that two functional circuits 3 have the same phase every time the counter signal counts a multiple of 6, and stores the value (i.e. 6 in this example) in a memory circuit. Configuring functional circuits 3 to make an attempt to communicate, then, can result in successful communication between them. This configuration can be realized with simple components including memory circuits and logical circuits, and the realization is possible by a person skilled in the art with reference to the specification and drawings.

Accordingly, Applicant respectfully submits that "how the second circuit supplies the first circuit with data when the counter signal has a value equal to a common multiple of n and m" is enabled and respectfully requests withdrawal of these rejections is respectfully requested.

Rejections under 35 U.S.C. § 102

Claim 9 stands rejected as anticipated by U.S. Patent No. 6,118,314 ("Arnould"). Applicant respectfully traverses this rejection.

Claim 9, as amended, recites a semiconductor integrated circuit device comprising: a semiconductor substrate having a first area and a second area; a plurality of counters one of which is provided in the first area and the second area and which cyclically count a same value at a same timing and output a counter signal as a result of counting; a first circuit provided in the first area, supplied with a first counter signal from the one of the counters in the first area and outputting a first signal when the first counter signal has a first value; and a second circuit

provided in the second area, supplied with a second counter signal from the one of the counters in the second area and supplying the first circuit with a second signal containing information on a value of the second counter signal obtained upon reception of the first signal.

Thus, one embodiment of the present invention includes that a first circuit outputs a first signal, a second circuit receives a second counter signal, and the second circuit provides the first circuit with a second signal containing a specific value.

Arnould et al. (US 6,718,314) discloses that a counter signal is supplied from a counter in a first area to a first circuit in the first area, and a counter is provided in a second area.

However, Arnould does not disclose that a second counter signal is supplied to a second circuit. The Examiner states that the second circuit as recited in Claim 9 corresponds to the reset generation circuitry 26 of Arnould and a counter signal is supplied to the reset generation circuitry 26 (See, Official Action, page 4, lines 20- 24). However, Applicant respectfully submits that it seems as if no counter signal is supplied to reset generation circuitry 26 as stated by the Examiner.

Arnould also does not disclose a second circuit providing a first circuit with a signal. The Examiner states that the first circuit as recited in Claim 9 corresponds to flip-flop 27 in master divider 24 of Arnould (See, Official Action, page 4, line 20), the second circuit of Claim 9 corresponds to reset generation circuitry 26 of Arnould as noted above, and the second signal of Claim 9 corresponds to signal 17 of Arnould (See, Official Action, page 5, line 1).

Applicant respectfully submits that Arnould does not disclose that the second circuit provides the first circuit with a signal as stated by the Examiner because reset generation circuitry 26 does not supply signal 17 to flip-flop 27 but to instead supply signal is supplied to reset detection circuitry 30.

Additionally, Applicant notes that the Examiner states that first circuit of Claim 9 corresponds to flip-flop 27 in master divider 24 of Arnould as mentioned above. However, the Examiner also states that the first circuit of Claim 9 corresponds to flip-flop 27 (which is apparently mistakenly referred to with the reference numeral "26" in the Official Action) in slave divider 34

of Arnould (See, Official Action, page 5, line 18). Applicant respectfully submits that the Examiner's use of flip-flop 27 in master divider 24 as the first circuit as recited in Claim 9 and the flip-flop in slave divider 34 as the first circuit as recited in Claim 9 is inconsistent and undermines the Examiner's assertions with respect to other limitations of Claims 9 as discussed above.

Moreover, even if the first circuit of Claim 9 is assumed to correspond to flip-flop 27 in slave divider 34, Arnould still does not disclose that a second circuit provides a first circuit with a signal because reset generation circuitry 26 supplies signal 17 to reset detection circuitry 30 as mentioned above, not to flip-flop 27 in slave divider 34.

Accordingly, it is respectfully submitted that Arnould does not disclose all limitations of Claim 9 and Application respectfully requests that the rejection of Claim 9 be withdrawn.

Claim Objections

Claims 7 and 8 stand currently objected to as dependent upon a rejected base claim but would be allowable if rewritten in base form. Applicant thanks the Examiner for the allowable subject matter. Applicant believes that rejected dependent Claim 6 is now in condition for allowance, and therefore respectfully requests the withdrawal of the objection to dependent Claims 7 and 8.

Conclusion

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 6-10. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

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